Emerging Nanoelectronic Devices

Instructor: Dr. Aaron D. Franklin, *Associate Professor in ECE & Chemistry*
Email: aaron.franklin@duke.edu
Office Hours: Tuesday & Thursday, 10am – 11am, CIEMAS 3473
Class Time & Location: Tuesday & Thursday, 8:30am – 9:45am, Hudson Hall 222
Course Website: http://piazza.com/duke/fall2014/ece59008/home (for Q&A, discussions, files, etc.)
TA: Erich Radauscher (erich.radauscher@duke.edu)
Prerequisites: understanding of semiconductor device physics

Course Description:
After a brief review of semiconductor device physics this course will cover the most prominent emerging nanoelectronic devices. The course will be divided into two parts: 1) nanoelectronic logic devices and 2) nanoelectronic memory devices. Logic devices that will be covered include advanced silicon transistors, carbon nanotube transistors, spintronics, 2D FETs, NEMS, tunnel FETs, and piezoelectronics. Memory devices include phase change, spin transfer torque, nanomechanical, ferroelectric FET, and molecular memory. Through this course, students will understand the basic operation, pros/cons of performance, and primary integration challenges for these emerging devices. A case study project will be included to improve students' ability to understand and extract information from journal papers through evaluation of a chosen nanoelectronic device, culminating with a presentation of their analysis to the class.

Objectives:
Through this course the students will:

- Refresh knowledge of semiconductor device physics related to conventional MOSFETs, with brief review of DRAM and SRAM memory.
- Understand various higher order effects (*e.g.*, short channel effects, quantum effects, discrete dopants, etc.) and how they influence the emergence of certain nanoelectronic devices.
- Understand the basic operation, pros/cons of performance, and major obstacles of integration for some of the prominent nanoelectronic logic and memory devices.
- Improve ability to efficiently evaluate journal articles on nanoelectronic devices.
- Demonstrate acquired skills in assessing a nanoelectronic logic or memory device by completing an in-depth evaluation on benchmarking of key metrics for a chosen device, culminating in a brief write-up and presentation to the class.

Textbook: Primarily class notes and journal articles. Here are a few useful textbooks for reference:

- A. Chen (editor), *Emerging Nanoelectronic Devices*, John Wiley & Sons, 2014 (preprint).
- Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices, 2nd Ed.*, Cambridge University Press, 2009.
- S. Datta, *Quantum Transport: Atom to Transistor*, Cambridge University Press, 2005.
- S. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, 1981.

Grading Criteria:

Homework	50 %
Project	30 % (15 % write-up & 15 % presentation)
Final Exam	20 %

Communication:
All questions on homework, projects, lectures, etc. should be posted to Piazza for open discussion. It is ok for the post to be kept as "anonymous." If students email the professor with questions on the

homework or lecture, they will likely be asked to post the question to Piazza to be answered there for the entire class to access.

Homework:
A homework assignment will be given each week. The assignments are intended to help the student solidify the important basics of each principle or device that is covered. Some of the problems will require locating journal papers and extracting relevant information, while others will be analytical.

Attendance and Late Homework Policy:
Attendance to the lectures is crucial to succeeding in this course. Homework will be due each week and must be turned in at the beginning of class – late homework will not be accepting except with written approval from the professor (and even then, only once/student per semester).

Collaboration Policy:
Students are allowed to work collaboratively on homework only with each student completing their own assignment. In other words, a group of students can work on their homework at the same time, discussing approaches, but each student must complete the problems on their own assignment.

Project:
This project makes up 30 % of the course grade and will be a group project (3-4 students assigned per group) and the nanoelectronic device will be chosen by the group on a first-come first-serve basis (no more than one group per device). While we may have discussed the device in class (we don't have to have covered it), the group will need to do more extensive searching for the latest results in the field. A write-up that is in the format and length of an *IEEE Electron Device Letters* paper will need to be turned in that includes:

- Schematic of device structure illustrating the key operating principles
- Representative electrical data showing how the device works (*e.g.*, current-voltage curves)
- Discussion of the basic operation of the device and key variations thereof
- Table that benchmarks the key metrics (at least 3 metrics) of at least 5 recently reported experimental versions of the device from the literature, comparing these metrics to the industry state-of-the-art for the applicable field (logic or memory)
    - If the chosen device has not been experimentally demonstrated, speak to the instructor about how to modify this requirement
- Include in the table the metrics from one or more theoretical projections for how the device is anticipated to perform
- Discussion of the major challenges to realizing the device in a technology
- Citation of all referenced work, figures, etc.

It should be noted that an *IEEE Electron Device Letter* is <u>not lengthy</u>! This should be concise and to the point, giving the reader a quick, yet sufficiently representative, overview of the device. Finally, we will take one lecture near the end of the semester for each group to present to the class the results of their benchmarking study. Each presentation will be allotted 10 minutes, with each group member presenting some portion, and then 5 minutes at the end will be given for the class to ask questions. The presentation should not simply be a display of the figures from the write-up, but should make use of the presentation environment to teach the class about the device, how it works, and what the current status is for the field. If there are any questions about the project, do not hesitate to ask the instructor.

Final Exam:

The final exam will essentially be a sanity check for all who have consistently attended the lectures. The problems will be very much like the homework problems, so that any student who has completed (and understood) all of the homework should be very familiar with what to expect on the final. The final will either be open note, or all needed equations will be provided.

Academic Integrity:

Academic integrity is expected as part of the community to which you belong and each student will be held accountable for upholding the standard. University policy will be enforced in the case of any dishonest conduct.

Anticipated Course Outline:

Week 1: Semiconductor device physics refresher

- Energy bands, density of states, p-n junctions
- Operation of a MOSFET
- Overview of DRAM and SRAM operation

Week 2: Scaling of MOSFETs

- Moore's law & Dennard scaling rules
- Voltage and power scaling dilemma
- Short channel effects and doping issues

Week 3: Keeping pace with the fast-moving field of nanoelectronics

- Which journals matter?
- ToC alerts, RSS feeds, etc.
- Finding, sorting, and citing papers

Week 4: Novel silicon & III-V devices

- ETSOI, FinFETs ("3D transistor"), and nanowire FETs
- III-V MOSFET, MISFETs

Week 5: Tunnel FETs

- Tunnel FET low power motivation
- Tunnel FET operation and examples

Week 6: Carbon nanotube FETs

- Carbon nanotube (CNT) properties
- CNTFET operation and material challenges

Week 7: 2D FETs

- 2D materials and properties
- 2D devices and operation

Week 8: NEMS and piezoelectronics

- NEMS motivation and examples
- Piezoelectronics background and basic devices
- Important tie between device & architecture

Week 9: Spintronics

- Intro to spintronics with example device

- Discussion on MOSFET-mimicking computing devices

Week 10: Memory device roadmap and phase change memory
- On-chip vs. off-chip memory
- Roadmap for memory devices
- Phase change memory operation and examples
- Advanced memory devices

Week 11: Project discussions and preparation work

Week 12: Project presentations

Week 13: Future of nanoelectronic devices
- Summarize key metrics
- What drives discovery? Invention?
- "Other" electronics
- Create your roadmap